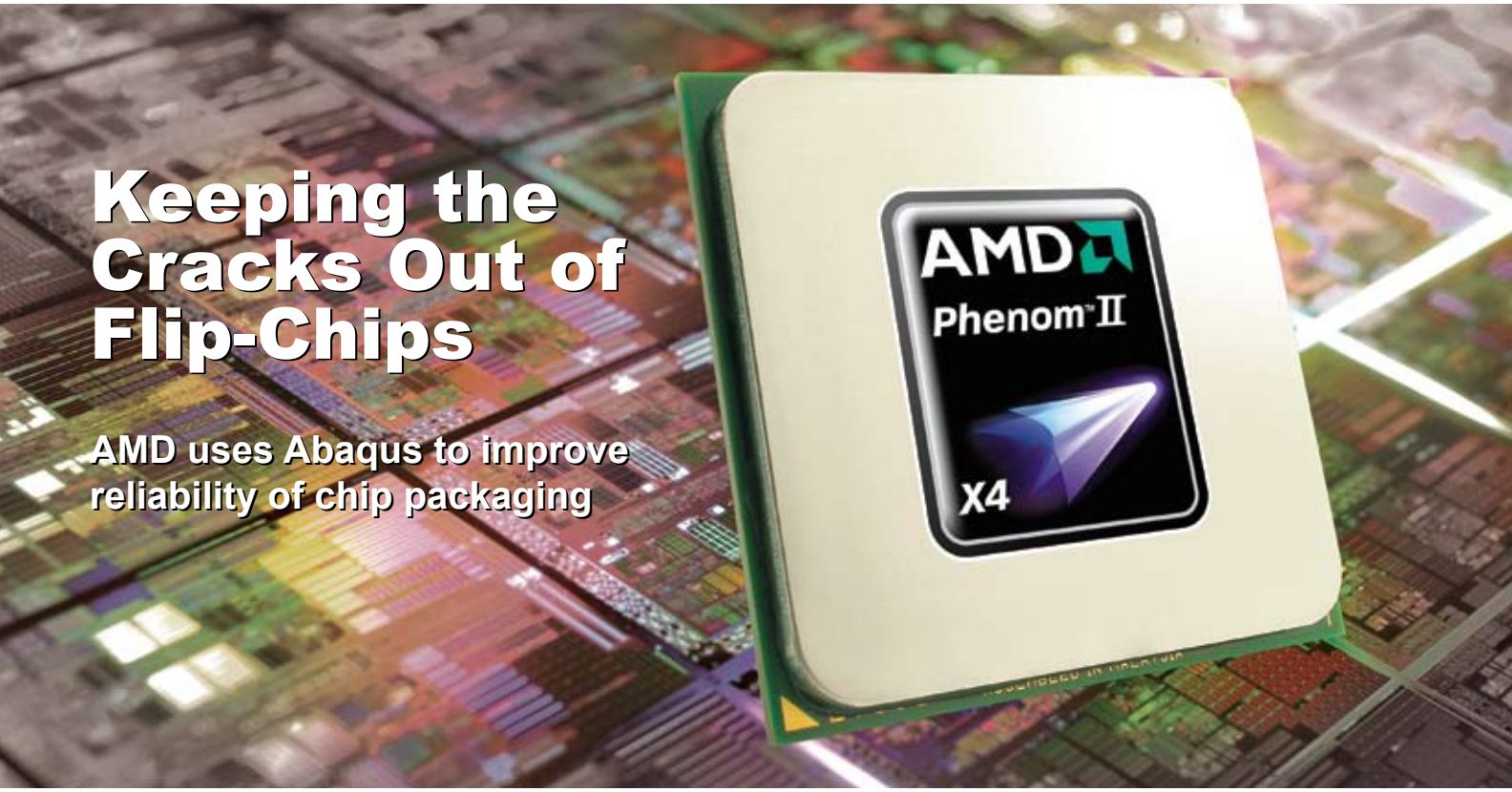

Keeping the Cracks Out of Flip-Chips

AMD uses Abaqus to improve reliability of chip packaging

Fifty years after its invention, it is hard to imagine life without the integrated circuit (IC). As the heart—or the brain—of all computers, ICs power the world's most complex systems in communications, manufacturing, and transportation. According to the Semiconductor Industry Association, the overall worldwide market for semiconductors was a healthy $248 billion in 2008. A significant and growing part of this market is the flip-chip.

Developed in the 1960s by IBM and used initially in mainframes, flip-chips are mounted face-down, or flipped, directly onto a substrate, circuit board, or carrier. They make an electrical connection with the surface on which they are mounted through precisely positioned bumps—tiny spheres of conductive material—which also allow heat to dissipate from the chip, act as a spacer between the chip and the board or substrate circuits, and provide mechanical support for the chip (see Figure 1).

Compared to their wire-bonded cousins, flip-chips have a number of significant advantages:

- size – they are small and can reduce circuit board area by up to 95 percent;
- performance – they have improved speed;
- cost – they are less expensive in high volumes;
- reliability – they are more rugged.

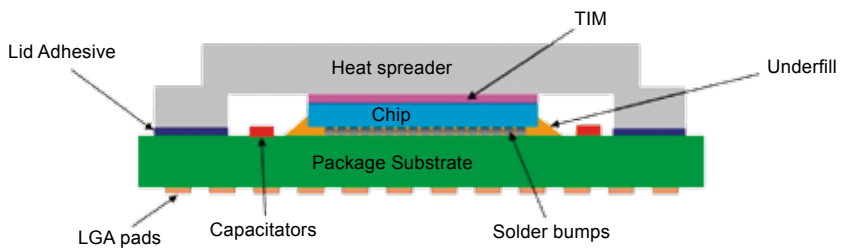

Figure 1. Schematic of generic flip-chip. The flip-chip faces down and is typically attached via solder bumps to the printed package substrate or circuit board. The underfill layer locks the die, or chip, to the substrate layer, protecting the bumps and improving durability.

Because of these advantages, flip-chips have become the chip-of-choice for many portable, cost-conscious applications such as watches, smart cards, RFID tags, cellular telephones, and pagers. And while it's been reported that more than one billion devices a year are manufactured using flip-chips, like any enabling technology, flip-chips still have their design and manufacturing challenges, and reliability improvements are still possible. It's no surprise, therefore, that finite element analysis (FEA) is being used in the ongoing development and improvement of chip design.

Preventing Underfill Failure is Critical

"In flip-chip packages, the mismatch in coefficients of thermal expansion (CTE) of the various layers induces stresses that can result in delamination," says Zhen Zhang, Senior Packaging Engineer at Advanced Micro Devices (AMD), a global supplier of integrated circuits for personal and networked computing and communications, based in Sunnyvale, CA. Especially critical is the underfill, a layer of adhesive between the chip and substrate that locks together the two layers. Once locked, the electrical contact is maintained, the contact bumps are protected from moisture and other environmental hazards, and the assembly has added mechanical strength.

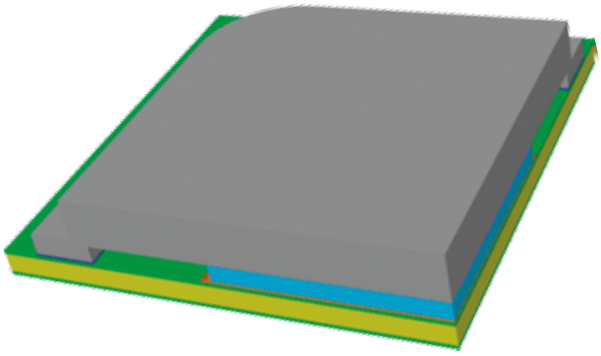

Figure 2. View of a 3D FEA model of a flip-chip. Only a quarter of the flip-chip is modeled because the flip-chip has symmetric geometry, loading conditions, and boundary conditions.

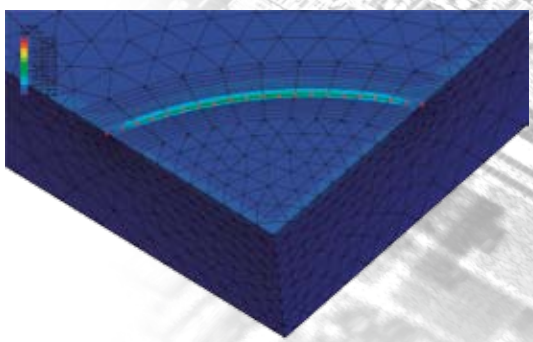

Figure 3. FEA analysis showing the stress field at the crack front.

Typically, a high modulus epoxy is used to underfill this gap and is applied by capillary flow and followed by a heat-curing step. While providing a number of advantages, the underfill layer can also have an impact on package reliability. "For instance, imperfect underfill with voids or microcracks will produce delamination under temperature cycling conditions," Zhang notes.

To help predict and prevent delamination, the engineering team at AMD used Abaqus finite element analysis software. They designed their study to analyze the effect of various underfill design variables that could potentially play a role in crack formation and delamination: the material modulus, CTE, and the dimensions of the underfill layer (fillet height). "We chose Abaqus because of its powerful fracture mechanics capabilities," says Zhang. "In addition, it has other features—such as contact mechanics, global-local submodeling routines, surface-to-surface tie constraints, a variety of partition and meshing tools, and parametric GUI and Python scripting for high productivity—all of which were useful in this study."

FEA Models Help Examine Underfill Behavior

To study delamination, engineers at AMD used Abaqus to create a parametric model of the flip-chip having the capability of automatic crack generation. The model included a base substrate layer (40 mm wide and 1.4 mm thick), a flipped silicon chip (20 mm wide and 0.8 mm thick) on top of the substrate, and an epoxy underfill layer between the substrate and chip (20 mm wide, 0.09 mm thick). In addition, the model included a copper heat-spreader lid that sits on top of the chip itself, gel-like thermal interface materials (TIM) between the chip and lid, and as the very top layer, adhesive for bonding the lid with the package substrate. To save on compute time, and because the geometry and loading conditions are symmetric, the team only modeled a quarter of the flip-chip (see Figure 2).

For the model's material properties, Zhang and his co-workers assumed that all materials were isotropic and had linear elastic behavior. In running analyses, since temperature excursion or cycling is the cause of many failures, the group focused on this variable, using an excursion of 125 to 25 degrees C—from the glass transition temperature of the epoxy underfill to room temperature.

"I used Abaqus/CAE to build the models," says Zhang, who took full advantage of the software's flexibility and automation features. "I modified the journal files into Python scripts and defined the parameters—including geometries, material properties, and loading conditions —for fully parameterized studies. I also used scripting/automation in Abaqus/CAE to post-process the simulation results and output them into Excel files."

The AMD engineering team used both a global model method (26,000 elements) and a global-local method (approximately 19,400 elements in the global model and 18,200 elements in the local model). In both cases they used the C3D20R element, a 20-node quadratic brick. For hardware, Zhang used a Windows XP Pro 32-bit operating system in a workstation powered by an AMD Opteron dual-core processor and visualized using an ATI Radeon HD graphics card.

Simulation Provides 3D Fracture Results and Design Recommendations

For the purposes of this study, Zhang's group inserted a crack at the corner of the interface between the chip and the underfill layer and then examined the effect of a number of variables on crack generation—underfill material properties (modulus and CTE), the height of the underfill fillet, the shape of the crack front, and the size of the crack (see Figure 3). "This complex analysis was made manageable by the parametric capabilities of the Abaqus model," Zhang notes. To optimize reliability and durability, the team analyzed these variables in regards to crack formation and came to the following conclusions about the underfill layer: the material should have a low CTE; the fillet height should be increased, if possible; the glass transition temperature of the material should be as low as possible, but should be higher than the upper bound of temperature range in testing or service condition; and the modulus effect is minimal.

Making Future Flip-Chips Even Better

Zhang, who has been studying flip-chips for two years, has already made significant recommendations and improvements in designs using FEA. "We have optimized solder joints, the contact reliability of the package bottom with the socket, and various package sizes for both single-chip and multi-chip modules—all using Abaqus." In this case, Zhang adds, "The analysis provided reliability data for all flip-chips in which underfill is incorporated—from package to board level, and from assembly to service conditions."

Looking to the future, Zhang notes that such analyses guide material selection and design and assembly optimization as well, and concludes, "The impact on future flip-chip design is positive." In a chip-driven world, this is good news.

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